Interleaved SCC-LCLC Converter with TO-220 GaN HEMTs and Accurate Current Sharing for Wide Operating Range in Data Center Application

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***Abstract*— In this paper, an interleaved LCLC converter with TO-220 enhancement mode GaN devices (e-mode GaN) and accurate current sharing performance is introduced for data center application. Any tolerance in the resonant tank elements can lead to large load imbalance between different phases. Due to the steep gain curve of LCLC converter, conventional current sharing methods are not so effective. In the proposed converter the impedances of the resonant networks are matched by switching a capacitor (i.e. Switch Controlled Capacitor SCC) in series with the resonant capacitor in one or some of the phases, which results in accurate load current sharing between phases (i.e. around 0.025% difference). The load share of each phase is sensed through the resonant current on each phase and the control logic is applied so current sharing between all phases can be achieved. By this method, an accurate current sharing is achieved for a wide input voltage range that is required for hold up time in data center application. Moreover, interleaving is applied in the proposed multi-phase LCLC converter resulting in low stress on the output capacitor allowing sole ceramic capacitor implementation. Moreover, phase shedding allows a flat high conversion efficiency curve for a wide load range. The performance of the proposed interleaved LCLC converter is verified by a two-phase 1 kW prototype with 250 V - 400 V input voltage and fixed 12 V output voltage.**

Keywords—Interleaved multi-phase resonant converter, current sharing, switch controlled capacitor (SCC), TO-220 e-mode GaN HEMTs, data center.

I. INTRODUCTION

In recent years, electrical demand of data centers has massively increased due to the fast development of information technology and cloud computing. Considering that data center services are still in a nascent stage, the power conversion capability should keep up with the growing electric demand. With advancements in power electronics technology more electric energy can be transferred to consumer loads in data centers. LLC resonant converters are widely used in data centers as a front-end converter to convert 400 V dc bus to 12 V for server motherboard low voltage bus due to their outstanding features such as zero voltage switching (ZVS) and zero current switching (ZCS) for power switches. The 12 V dc bus then is connected to point of load converters to supply CPU, memory and other chips [1]-[3].

In data center application it is required for dc-dc converters to be able to operate in wide input voltage range to provide power during hold-up time in case of ac line failures. It has been reported that LCLC resonant converter demonstrates an improved hold-up performance compared with an equivalent LLC resonant converter performance [3]. Another issue in data center application is high current level (e.g. 80A) at low voltage side bus (i.e. 12 V), which limit the power level of resonant converters used in data centers to 1 kW and less. Hence, it is required to parallel several resonant converters to distribute power stress and increase current capability. By implementing phase interleaving, the output filter of the resonant converter can be designed with a smaller capacitance. To benefit from interleaving in resonant converters, current sharing performance should be studied precisely because the capacitors and inductors used in the resonant tank have tolerances and the voltage gain of resonant converters varies based on the impedance of the resonant network. Thus, any small imbalance in the voltage gain of one phase can cause significant imbalanced current sharing among individual phases. Unequal loading of phases is a critical problem in interleaved resonant converters because it reduces converter efficiency, cause thermal imbalance and can lead to converter failure in severe load conditions.

Various passive and active current sharing methods have been proposed for multiphase LLC converters. In [4]-[7], different passive and automatic impedance matching (PIM) methods including common-inductor and common-capacitor approaches have been studied thoroughly for different resonant tanks. The PIM method is quite effective in current sharing as they do not require additional components and control scheme. However, the current sharing performance will be compromised when there are random positive and negative tolerances in all resonant components. Moreover, in most of the passive current sharing methods phase shedding cannot be implemented to increase light load efficiency.

In [8], a single integrated magnetic is used in a three-phase LLC converter to balance the current sharing. Like other integrated magnetic based methods, this method is not so effective in current balancing when the converter is operating in wide input voltage. In [9], a current sharing approach is performed for an interleaved LLC converter by adjusting the duty cycle of the phase that caries higher load share. Although,

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in this method only a new control method is needed, but the duty cycle cannot be reduced too much to compensate for large tolerances and converters with wide operating range. In [10] and [11], current sharing is done by adding one or two power switches in each phase to switch in and out a capacitance or inductance in the resonant tank to compensate the gain difference between phases. This method provides a precise way of adjusting current between phases at the expense of additional components. However, the additional power devices do not have any switching losses and there is only switch conduction loss, hence it does not compromise efficiency noticeably.

In this paper, the switch controlled capacitor (SCC) method has been implemented in a wide input voltage resonant converter as it is flexible to interleave any number of phases and implement phase shedding to improve efficiency profile. Moreover, for wide input range resonant converters, it is not efficient to do PCB windings for magnetics to achieve fixed inductances, hence SCC approach is a better solution than conventional methods that can handle large tolerances for an interleaved LCLC converter. The SCC technique has never been studied for any resonant converter with a steep voltage gain to investigate the accuracy of current sharing. In this paper, the half-wave SCC is implemented on both phases of a wide operating range two-phase LCLC converter.

The rest of this paper is organized as follows, in the next section the characteristics of different parts of the proposed SCC-LCLC resonant converter is analyzed, in Section III the control method and current sharing performance is discussed. In Section IV, practical considerations using GaN HEMTs is provided. Experimental results of a laboratory prototype are provided in Section V, and Section VI is conclusion.

II. The Proposed SCC-LCLC Resonant Converter

A. LCLC Resonant Conveter

As mentioned before, wide input voltage range is a desired feature for front-end DC-DC converters to satisfy required hold-up time especially in data center application. If variation of input voltage range is too large, the performance of LLC converter can be deteriorated. With LLC network a small magnetizing inductor is needed to meet the voltage gain requirement when input voltage is low, which will increase circulating current and primary side RMS current through magnetics and switches leading to increased power loss. To find a suitable solution for wide input voltage range, a modified LLC resonant converter called LCLC resonant converter is proposed in [3]. The LCLC resonant converter is consisted of two resonant inductors (L_r and L_p and two resonant capacitors (C_r and C_p) that is theoretically equal to an LLC resonant converter with changeable magnetizing inductance. The topology of a half-bridge LCLC resonant converter with full-wave rectifier is shown in Fig. 1.

The equivalent magnetizing inductor of LCLC resonant converter can be changed by changing the switching frequency. The desired magnetizing inductor is implemented by a series connected parallel inductor and parallel capacitor. The resonant components can be selected through the design procedure of the LCLC converter based on the input voltage range, output voltage and current as described in [3]. After the design procedure, the equivalent magnetizing inductor (L_{m_eq}) at different switching frequency can be calculated as

$$L_{m\_eq} = L_p - \frac{1}{(2\pi f_s)^2 C_p} \tag{1}$$

The voltage gain of the LCLC resonant tank can be calculated by substituting (1) in the voltage gain expression of LLC resonant tank as follows

$$M_{LCLC} = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_{m\_eq}} - \frac{L_r}{L_{m\_eq} f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{2}$$

where the series resonant frequency (f_r), normalized frequency (f_n), the equivalent output resistance of the LCLC converter transferred to the primary of the transformer (R_e) and the quality factor (Q) are as follows

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3}$$

$$f_n = \frac{f_s}{f_r} \tag{4}$$

$$R_e = \frac{8 \times n^2}{\pi^2} \times R_L \tag{5}$$

$$Q = \frac{\sqrt{L_r / C_r}}{R_e} \tag{6}$$

The voltage gain characteristics of LCLC and LLC resonant tanks are demonstrated in Fig. 2. In order to get the same switching frequency variation for a specific required voltage gain in both resonant tanks, a 70 µH magnetizing inductance is needed for the LLC resonant tank. However, the magnetizing inductance in the LCLC resonant tank can be higher than that of LLC tank and the equivalent magnetizing inductance is changeable. When the input voltage is high, the required voltage gain is low, hence the switching frequency can be designed to be around around the resonant frequency, in this case the magnetizing inductance is large. Hence, the primary side RMS current can be reduced compared to an equivalent LLC converter. On the other hand, When the input voltage is low, the required voltage gain is high, hence the switching frequency is low and near the parallel resonant frequency, which in this case the magnetizing inductance is small to allow high voltage gain. From Fig. 2 it is clear that the voltage gain curve of LCLC

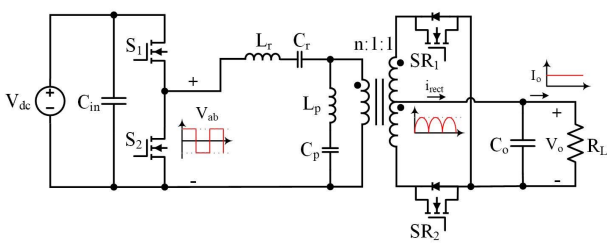


Fig. 1. The schematic of LCLC resonant converter.

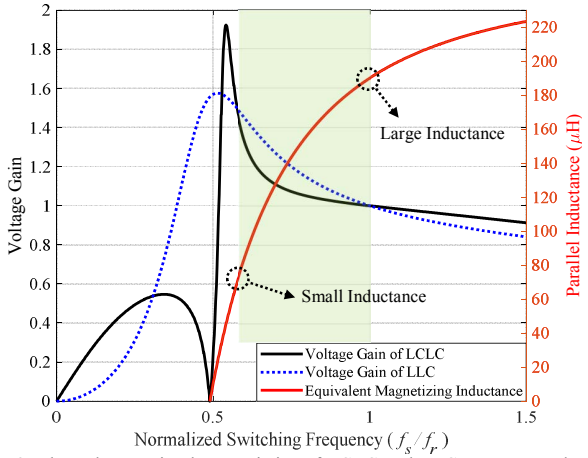


Fig. 2. The voltage gain characteristics of LCLC and LLC resonant tanks along with the changeable equivalent magnetizing inductance for LCLC resonant tank.

resonant tank is much steeper than of the voltage gain curve of LLC resonant tank. Hence, the variation of the voltage gain is more sensitive to the variation of the switching frequency in LCLC converter. The latter makes the current imbalance problem due to the resonant tank element tolerances of LCLC resonant converter worse than that of LLC resonant converter. Hence, in order to actively and accurately tune the voltage gain, a switch controlled capacitor can be implemented to solve the current sharing problem.

B. Half-Wave SCC

The half-wave SCC circuit consists a capacitor C_a in parallel with one MOSFET, S_a, as shown in Fig. 3. Switch S_a is connected to a low side driver as it shares a common source with main bridge switches.

Fig. 4 shows the half-wave SCC operation waveform. The operation principle of the SCC circuit is described as follows. Assuming a sinusoidal current I_{AB} is flowing through SCC and the current zero-crossing points are at angle 0, π, 2π, … etc. Switch S_a is turned OFF at angle 2nπ+α. After S_a is turned OFF, the current flows from A to B via C_a and charges the capacitor until the next current zero-crossing point at (2n+1)π. Then, the current reverse direction, and begins to discharge C_a. After C_a is fully discharged, the negative current is about to flow from B to A via the body diode of S_a. To prevent its body diode from conducting, S_a is turned ON. It remains ON for the rest of cycle and turns OFF again at angle (2n+2)π+α.

The equivalent capacitance of SCC, C_{SCC} is modulated by the delay angle α and can be expressed as,

$$C_{SCC} = \frac{2C_a}{2-(2\alpha - sin2\alpha)/\pi} \tag{7}$$

where, Ca is the SCC parallel capacitor. The equivalent series resonant capacitance ($C_s = C_{SCC}||C_r$) can then be derived as,

$$C_s = \frac{2C_aC_r\pi}{2C_a\pi + 2C_r\pi - 2C_r\alpha + C_r sin2\alpha} \tag{8}$$

where, C_r is the resonant capacitor of the original tank.

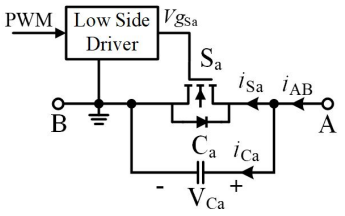


Fig. 3. The structure of half-wave SCC circuit.

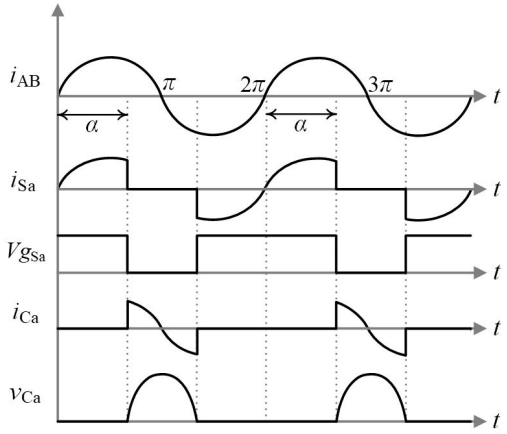


Fig. 4. General waveform of half-wave SCC with sinusoidal current.

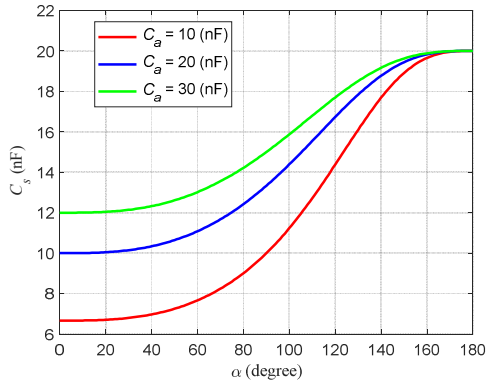


Fig. 5. The variation of the series resonant capacitance (C_s) due to the change in angle α (C_r=20 nF).

The angle α is changing from 0 to π, which is corresponding to the minimum and maximum resonant capacitance. When α = 0, current I_{AB} will flow through C_a and bypass SCC MOSFET. Thus, the equivalent resonant capacitance is at the minimum value which is equal to C_r and C_a connected in series. When α = π, current I_{AB} will flow through SCC MOSFET and bypass capacitor C_a, which makes the equivalent resonant capacitance toward to its maximum value C_r. In other word, SCC can change the equivalent resonant capacitor by varying the delay angle α so as to compensate the tolerance through reducing equivalent series resonant capacitance C_s.

C. Interleaved SCC-LCLC Resonant Converter

Fig. 6 shows the schematic of the two-phase LCLC converter with SCC circuit implemented on both phases. By employing SCC on both phases, any random imbalance can be compensated by both SCC circuits and a reliable performance can be

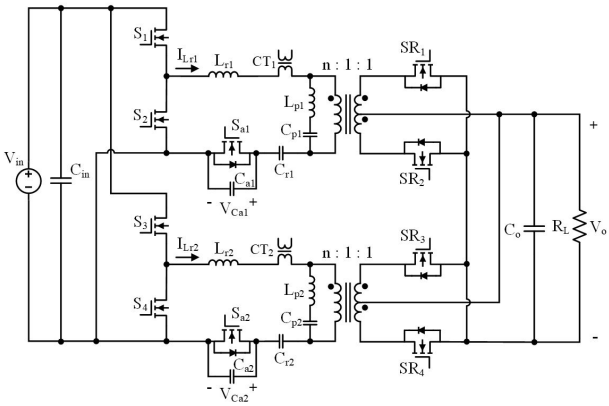


Fig. 6. The proposed interleaved SCC-LCLC resonant converter.

achieved. Switches S_{a1} and S_{a2} are half-wave SCC MOSFETs that switch in and out SCC capacitors (i.e. C_{a1} and C_{a2}) to compensate the resonant current by achieving an equal voltage gain with the same switching frequency for both phases. Two current transformers (i.e. CT_1 and CT_2) are used for current zero crossing detection that is required for the synchronization of SCC gate pulse for each phase as well as resonant current measurement that is require for current sharing performance and SCC gate pulse generation (α_1 and α_2). All these data will go into an MCU and correct gate pulse will be generated for SCC MOSFETs. More details of the control strategy and SCC operation are provided in the next section.

III. Control and Current Sharing Performance of the SCC-LCLC Converter

In the SCC-LCLC converter the resonant current of each phase is sensed by a current transformer to find out the level of load that is shared among different phases. Then, based on the control algorithm that is shown in Fig. 7, the proper command to increase or to decrease the angle α of each phase is produced in the MCU. In order to reduce the effect of SCC operation on the original LCLC converter, it is desired to increase the angle α of the higher current phase first and then to decrease the angle α of the other phase. In order to turn ON the SCC MOSFET at the right time it is necessary to find out the Zero-Current Crossing (ZCC) point of the resonant current, which can be implemented by the same current transformer that is used for current level measurement. The output voltage of the SCC-LCLC converter is regulated by a frequency-controlled PI loop. The basic waveforms of the SCC-LCLC converter including the operation of SCC is shown in Fig. 8. In this waveform it is considered that the load share in phase 2 is lower than phase 1 and more SCC compensation is required for phase 2.

In resonant converters when the load is changed the voltage gain characteristic curve changes and hence the RMS current of the resonant current changes. Thus, in order to see the effect of changing angle α on the current sharing performance, the RMS value of the resonant current of all phases can be investigated. For simplicity it is considered that the operating point is at resonant ($f_s = f_r$) and the resonant inductor current is pure sinusoidal. The resonant current can be written as follows

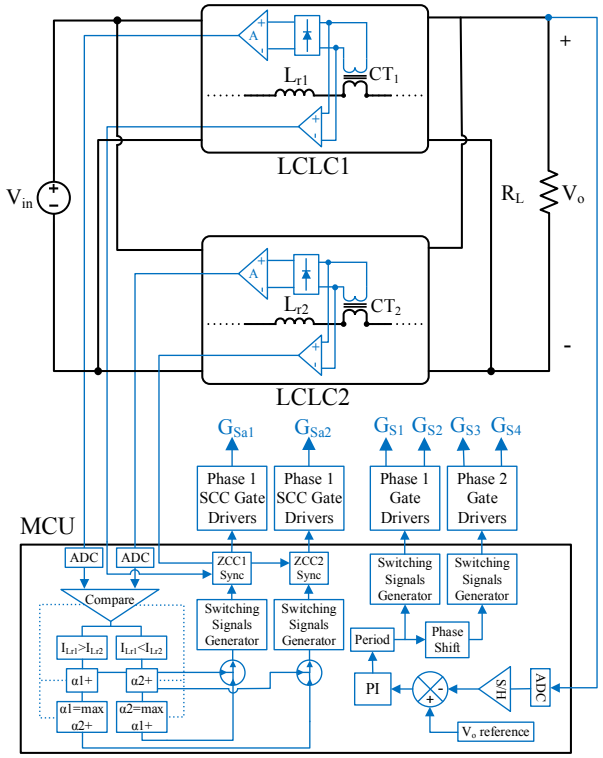


Fig. 7. The control scheme of the proposed SCC-LCLC converter.

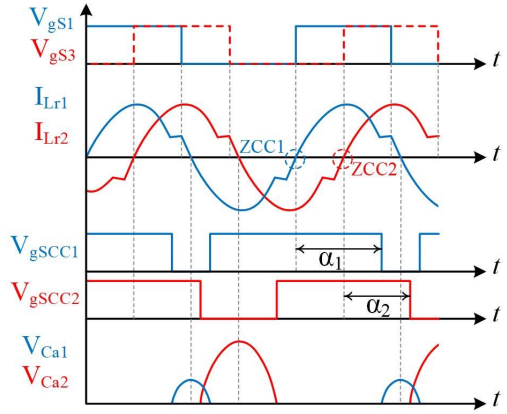


Fig. 8. Key operational waveforms with SCC.

$$i_r(t) = \sqrt{2} I_{Lr\_RMS} \sin(2\pi f_s t - \phi) \tag{9}$$

where I_{Lr_RMS} is the resonant RMS current.

The magnetizing current can be written as follows

$$i_m(t) = \begin{cases} -I_{m\_max} + \dfrac{nV_o}{L_{m\_eq}} t \\ I_{m\_max} - \dfrac{nV_o}{L_{m\_eq}} (t - \dfrac{T}{2}) \end{cases} \tag{10}$$

The peak value of the magnetizing current can be calculated as follows

$$I_{m\_max} = \frac{nV_o T}{4L_{m\_eq}} \tag{11}$$

To comply with the assumption made at the beginning of analysis, the equivalent magnetizing (L_{m_eq}) inductance should be calculated at the resonant frequency in above equations. The RMS resonant current can be calculated from the amount of energy transferred to the load as follows

$$I_{Lr\_RMS} = \frac{V_o \sqrt{4\pi^2 + n^4 {R_L}^2 \left(\frac{1}{L_{m\_eq} f_s}\right)^2}}{4\sqrt{2} n R_L} \quad (12)$$

By changing angle α on any phase, the equivalent resonant capacitor in that phase will change and hence the voltage gain and output voltage change, and so does the resonant RMS current. Thus, using (2) the relationship between the resonant current and resonant components can be expressed in (13).

As shown in Fig. 5 small values of SCC capacitor and small delay angles of α can change the series resonant capacitance a lot leading to a significant change in the resonant frequency of half-cycle, which can adversely affect the performance of the resonant converter by making it too much asymmetrical. Asymmetrical operation is not desirable in resonant converters as it can reduce the turn ON time of only one leg of input switches and SRs and hence increase the power loss and decrease the conversion efficiency. Therefore, small values of α should be avoided and in practice a moderate value of α between 100° to 170° is desirable. In Fig. 9 the effect of changing the switching frequency and delay angle α in the resonant current is depicted. As can be seen the variation of resonant current is the largest when SCC compensation is relatively large (~ α=100) and switching frequency is low (i.e. near peak gain).

In order to see the accuracy of current sharing, the effect of the smallest change in α can be observed on the resonant RMS current change. Using the design method proposed in [3] for the input parameters of V_{in_min} =250 V, V_o =12 V, P_o =500 W, f_{s_min} =175 kHz, the following parameters can be selected L_r=12 uH, C_r=20 nF, L_p=230 uH, C_p=5 nF and n=18 for the power circuit of LCLC converter, and C_a =20 nF and $\alpha_1 = \alpha_2$=100° are used for the SCC circuit to have a large enough compensation range. With 1 ns change in duty cycle, delay angle α varies by 0.066°. So, the smallest change in α only for phase two leads to α_2=100.066° and then the RMS current difference ($\Delta_{I_{Lr}}$) can be calculated using (13) as follows

$$\Delta_{I_{Lr}} = I_{Lr2\_RMS} - I_{Lr1_{RMS}} \xrightarrow{\substack{I_{Lr1_{RMS}}=3.3922 \\ I_{Lr2_{RMS}}=3.3932}} \Delta_{I_{Lr}} = 0.001 \text{ A} \quad (14)$$

Hence, the maximum accuracy in current sharing by this method using a 16 bits MCU is around 0.028%. A simulation setup in built in PSIM using the same parameters used for calculation to compare the accuracy of the calculation. The resonant current waveforms and the RMS values are shown in

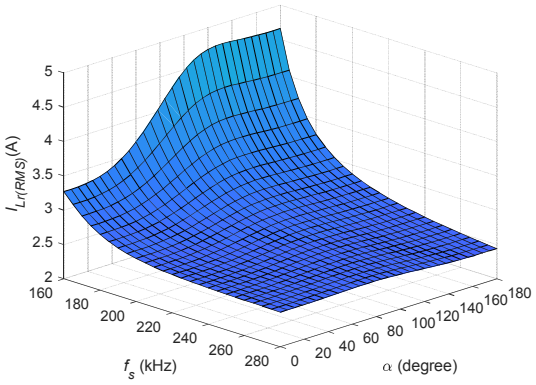


Fig. 9. A 3D plot of the resonant RMS current variation due to the change in switching frequency (f_s) and angle α (with C_a=20 nF).

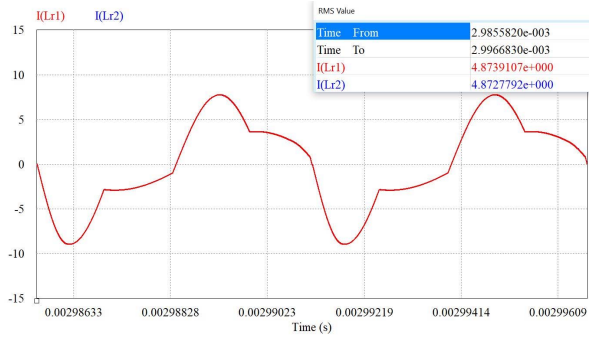


Fig. 10. The simulated result for the resonant RMS current.

Fig. 10. The difference in resonant RMS current from the simulation is $\Delta_{I_{Lr}}$ =0.00113 A and the accuracy of current sharing can be calculated as 0.023%. The difference between the RMS values taken from the calculation and simulation is because of first harmonic approximation in analytical calculations that leads to inaccuracy at frequencies below the resonant frequency.

IV. Practical Implementation Consideration using GaN HEMT Devices

Switching devices are playing a key role in designing new high efficiency converters for datacenter application. GaN HEMTs have small gate charge (G_g) and output capacitance (C_{oss}) compared to typical Si devices. GaN devices demonstrate various benefits in high frequency soft-switching resonant converters from several aspects. In general, a large enough deadtime is required for switches to achieve ZVS in resonant converters. Increasing the deadtime reduce the effective turn ON time of the switch in a cycle and hence increase the RMS current through the switch and magnetic windings, which can increase power loss. On the other hand, by increasing the switching

$$I_{Lr\_RMS} = \frac{V_{in} \sqrt{4\pi^2 + n^4 {R_L}^2 \times \left(\frac{1}{L_{m\_eq} f_s}\right)^2}}{8\sqrt{2} n^2 R_L \sqrt{\left(1 + \frac{L_r}{L_{m\_eq}} - \frac{L_r}{L_{m\_eq}} \times \frac{1}{4\pi^2 L_r C_s f_s^2}\right)^2 + \frac{L_r}{C_s} \times \left(\frac{\pi^2}{8n^2 R_L}\right)^2 \left(2\pi\sqrt{L_r C_s} f_s - \frac{1}{2\pi\sqrt{L_r C_s} f_s}\right)^2}} \quad (13)$$

frequency the deadtime need to be reduced and hence a higher magnetizing current is required to achieve ZVS, which requires for a smaller magnetizing inductance. This will increase circulating current and power loss. By using GaN HEMTs a small deadtime can be used with larger magnetizing inductance and smaller air gap and less fringing loss in the windings, which is because GaN switches can turn ON and OFF much faster than Si switches. Moreover, the fact that GaN devices do not have body diode makes them a perfect choice for resonant converters in light load conditions, which is because of little to zero reverse recovery loss and no requirement for deadtime expansion in light load to maintain ZVS operation [12] and [13].

In earlier generation of GaN devices, many manufactures have used Depletion-mode (D-mode) GaNs in cascode structure to make a normally OFF device, which is realized by a series connection of a low voltage Si FET and a high voltage D-mode GaN HEMT. This configuration is motivated by a reasonably high threshold gate voltage, small output capacitance, low reverse recovery charge and conventional TO package with good thermal performance and ease of use. However, cascode configuration compromises the superior performance of single device GaNs. Recently, Enhancement-mode (E-mode) GaN devices are widely used by manufacturers and researchers around the world due to their superior performance like high transition speed, low drain source turn-ON resistance and reverse conduction with no reverse recovery. Most of the E-mode GaN HEMTs come in surface mount small packages from different manufacturers. Although, the small packaging can bring low parasitic inductance, the thermal performance is a critical issue specially for high power applications [12]-[14]. Recently, E-mode GaN devices with TO package is manufactured to take advantage of all benefits of surface mount GaNs as well as better thermal management due to the metal tab that is available for heatsinking. Because of additional Si FET in cascode GaNs, the parasitic package inductance of both surface mount and through-hole packages are higher compared to E-mode GaNs. Nowadays, E-mode GaNs are the mainstream Wide Band Gab (WBG) switching devices in the industry due to their superior performance over other WBG devices.

Among all parasitic components, common source inductance (CSI) that is shared by both driving loop and power loop is the most significant one because of its direct effect on gate driving performance and consequent power loss or gate breakdown [14]. During the presence of high di/dt a voltage will be created on CSI that can reduce the gate to source voltage and hence prevent optimal use of fast switching capability by slowing down the switching time. This is very important in hard-switching converter as the switching loss is directly affected by the switching speed. In resonant converters, ZVS operation is always sought at turn-ON, and during deadtime when the GaN is in reverse conduction the negative current level is usually low as a marginal ZVS operation design is always considered to reduce circulating RMS current through the circuit. Hence, there is no high di/dt during the actual turn-ON transition and the voltage drop on the gate is not noticeable. However, during turn ON an LCR resonant tank is formed between CSI, gate capacitance and gate resistance that should be damped in order to avoid positive voltage ringing across the gate (see Fig. 11). The voltage ringing can pass the threshold voltage and cause

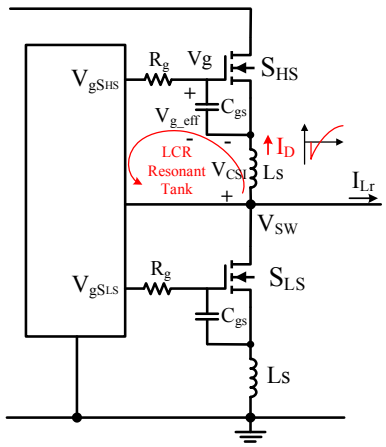
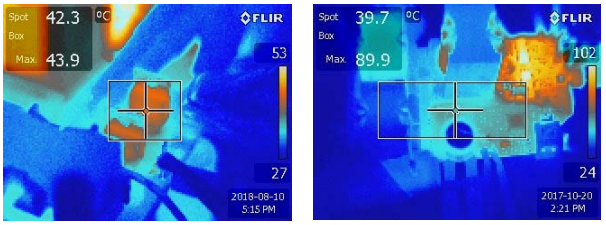


Fig. 11. The effect of CSI on gate drive performance.



(a) TO-220 15 A ($R_{DS(on)}$=92 mΩ) (b) GaN*px*™ 60 A ($R_{DS(on)}$=25 mΩ)

Fig. 12. Thermal images of different GaN packages for full load condition.

shoot-through by unwanted turn ON of the GaN. This can be alleviated by increasing the damping effect either by increasing the gate resistance or adding a small ferrite bead to the gate.

$$V_{g\_eff} = V_g - V_{SW} + L_S \times \frac{dI_{DS}}{dt} \tag{15}$$

In this study, 650V E-mode GaN HEMTs in TO-220 package from GaN Power International [15] are used in a 500W LCLC resonant converter and compared with a GaN*px*™ package from GaN Systems in the same design [16]. In the test setup only air stream cooling is used for thermal dissipation and no heat sink is used for the GaN devices. The current rating of the implemented GaNs with TO-220 package is 15 A and the current rating of the GaN*px*™ package is 60 A. The thermal images of both GaN devices are shown in Fig. 12 with 400 V input voltage and 12 V output voltage at 40 A load. As can be seen the temperature of both GaNs is around 40 degree with fan cooling. It is deemed that using surface mount GaNs may lead to overdesign in order to reduce condition loss to meet the same heat dissipation requirement as in an otherwise-identical design with through-hole GaNs. Hence, if the resonance on the gate voltage is properly alleviated, TO-220 GaN package is a good candidate for high power applications as the higher parasitic inductance of the TO packages is not a big concern in resonant converters because of ZVS switching and small di/dt at turn ON.

V. Experimental Results

A 1 kW experimental prototype has been built in the laboratory with the design parameters listed in Table I. The experimental setup with the device under test (DUT) at full load condition is demonstrated in Fig. 15. As E-mode GaN HEMTs with TO-220 package are used in the proposed converter, SCC MOSFET and Synchronous Rectifiers (SRs) are also with TO-

220 package in this prototype for consistency. It has been observed that the performance of through-hole SRs with TO-220 package is relatively similar to surface mount counterparts and the negative effects due to the higher output capacitance can be curbed using a small RCD noise filter [17]. Moreover, the magnetics are intentionally made with different values for both phases to count for severe imbalance condition. Fig. 14 shows the steady state resonant current with 400 V input voltage for both half-load and full-load conditions. As can be seen from Fig. 14 after applying the SCC circuit the resonant current is actively balanced among both phases for different load conditions. Because the layout of secondary side circuit physically does not allow a direct current measurement of the output current of each phase, the current sharing performance between the two phases are compared through the resonant current. The SCC capacitor voltage for both phases are below 20 V and it is larger in phase 2 to compensate current imbalance.

TABLE I. THE PARAMETERS USED IN THE PROTOTYPE

Description	Value
Input Voltage	250 – 400 VDC
Nominal Input Voltage	400 VDC
Output Voltage	12 VDC
Rated Output Current	80 A
Rated Output Power	1 kW
Switching Frequency	170 – 250 kHz
Transformer Turns Ratio	18 : 1 : 1 (center tapped)
Resonant Inductor (L_r)	13.4 µH (Phase1) - 12.5 µH (Phase2)
Parallel Inductor (L_p)	239 µH (Phase1) – 245.6 µH (Phase2)
Resonant Capacitor (C_r)	20 × 1 nF = 20 nF ± 5%
Parallel Capacitor (C_p)	5 × 1 nF = 5 nF ± 5%
SCC Capacitor (Each Phase)	5 × 3.3 nF = 16.5 nF ± 5%
Input Capacitor (Electrolytic)	2 × 68 µF = 136 µF ± 5%
Output Capacitor (Ceramic)	20 × 47 µF = 940 µF ± 5%

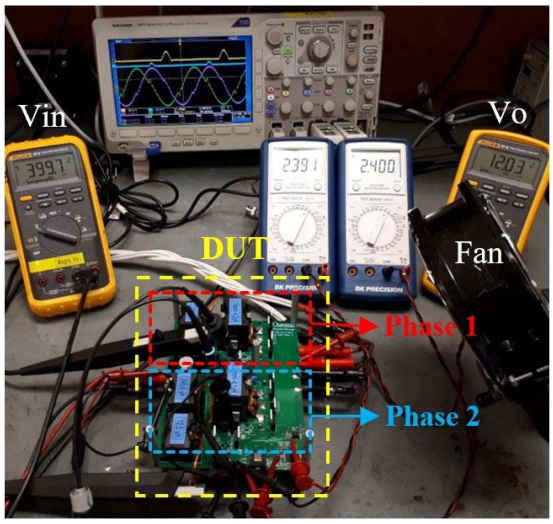


Fig. 13. Photo of the laboratory prototype under test.

Fig. 15 shows the steady state resonant current of both phases with 250 V input voltage and for half-load and full load conditions. It can be seen that the SCC capacitor voltage in phase 1 is larger in this case to compensate for the gain difference. The maximum SCC capacitor voltage is around 70 V in this case with 250 V input voltage and full load condition. The difference between the SCC capacitor for 400 V and 250 V input voltages is due to the larger gain difference at higher gain curves and lower switching frequencies that requires higher gain compensation for 250 V.

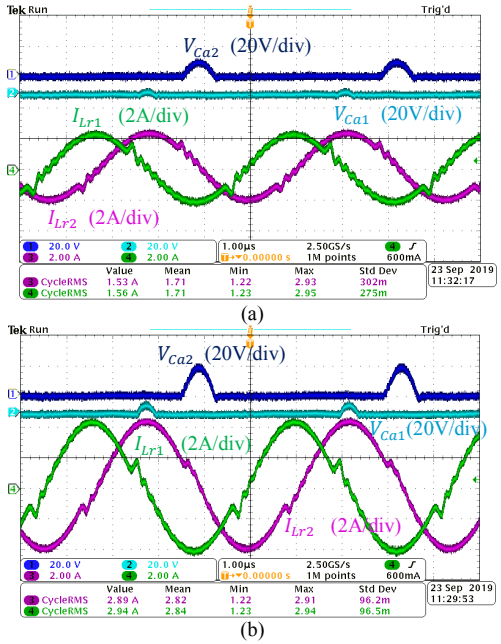


Fig. 14. The steady state waveforms with 400 V input voltage for (a) half-load (40 A) and (b) full-load (80 A) conditions.

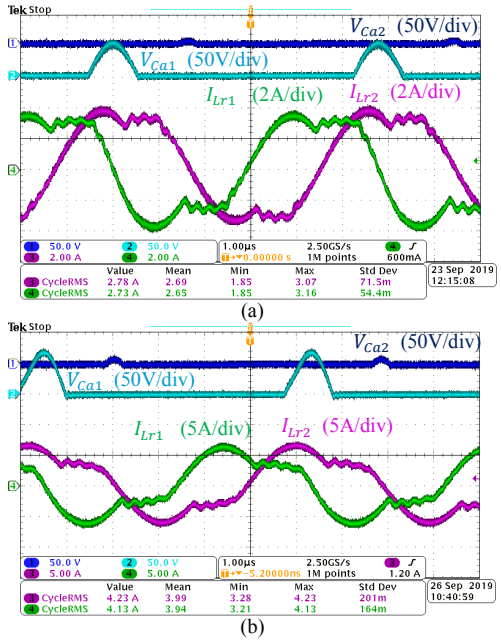


Fig. 15. The steady state waveforms with 250 V input voltage for (a) half-load and (b) full-load conditions.

Furthermore, the output capacitor voltage ripple and temperature are compared for interleaved and non-interleaved modes in Fig. 16. By applying 90º phase interleaving the output capacitor voltage ripple and the current ripple are reduced significantly. It can be seen that the output voltage ripple is reduced to less than half, and the output capacitor temperature (T_{Co}) is reduced from 61º to 46º for 400V input voltage condition. The reduction in output capacitor current ripple leads to the reduction of the power loss occurred in the output capacitor and hence efficiency increase. Fig. 17 shows the efficiency curve for 400 V input voltage with and without phase shedding. It is clear that the proposed converter can achieve a flat efficiency curve over a wide input voltage and load range with more than 96% efficiency from 15A to 80A load range and with the peak efficiency of 96.7%.

VI. Conclusion

This paper proposed an interleaved LCLC resonant converter with current sharing for a wide operating range. An accurate current sharing is achieved by implementing an SCC technology in both phases of an LCLC converter. With this method, the accuracy of current sharing can be as high as 0.025% in theory. The current sharing performance is verified through experimental results for half-load and full load conditions for both 250 V and 400 V input voltages. Moreover, the operation of the proposed converter is compared for non-interleaved and interleaved operations and it is observed that the output capacitor temperature is reduced by 15 degree by interleaving. The proposed converter achieved a flat efficiency curve over a wide load range with a peak efficiency of 96.7%.

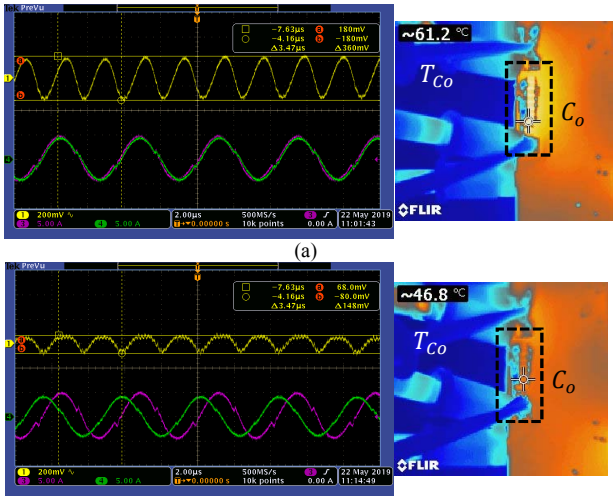


Fig. 16. Experimental results for resonant current waveforms, output capacitor voltage ripple and the temperature of output capacitor (T_{Co}).

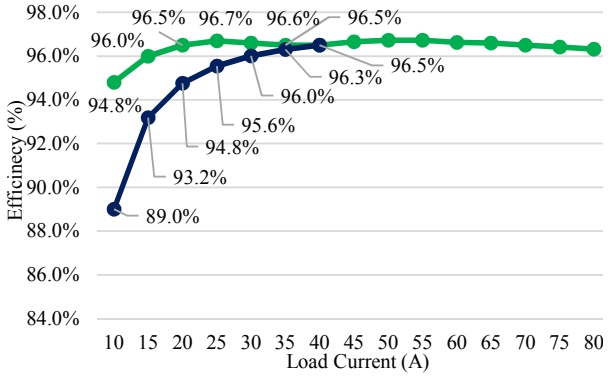


Fig. 17. Efficiency curve for 400 V input voltage with and without phase shedding over a wide load range.

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